**IN THE CLAIMS**

Please cancel claims 1-24 and add the following claims:

1-24) (Canceled.)

25) (New.) A method comprising:

providing a calibration value to a first digital-to-analog converter ("DAC"), coupled to an output, in a device;

outputting a first current from a second DAC in response to an initialization value; and,

providing a first bias current to the first DAC in response to the first current in order to provide an output current at the output.

26) (New.) The method of claim 25 wherein providing a first bias current comprises:

providing the first bias current to a transistor coupled to the first DAC.

27) (New.) The method of claim 25 further comprising:

obtaining a DAC value associated with the first DAC;

applying the DAC value to the second DAC;

outputting a second current from the second DAC in response to the DAC value; and,

providing a second bias current to the first DAC in response to the second current.

28) (New.) The method of claim 25 wherein the first DAC is a N-bit DAC, the second DAC is an M-bit DAC and the DAC value is an m most significant bits of the first DAC, wherein M is less than N.

29) (New.) The method of claim 25 wherein the device is a dynamic random access memory ("DRAM") device.

30) . (New.) The method of claim 25 wherein the providing a calibration value comprises providing the calibration value by a memory controller.

31) (New.) The method of claim 25 wherein the output is coupled to a pin.

32) (New.) A method for calibrating an output driver comprising:

providing a calibration signal, wherein the calibration signal is provided by a memory controller;

receiving the calibration signal, wherein the calibration signal is received by a memory device;

storing a calibration value in response to the calibration signal;

providing the calibration value to a first DAC, coupled to the output driver, in the memory device;

outputting a first current from a second DAC in response to an initialization value;

providing a first bias current to a transistor, coupled to the first DAC, in response to the first current; and,

providing an output current at the output driver in response to the first bias current.

33) (New.) The method of claim 32 further comprising:

obtaining a DAC value associated with the first DAC in the memory device;

applying the DAC value to the second DAC in the memory device;

outputting a second current from the second DAC in response to the DAC value; and,

providing a second bias current to the output driver in response to the second current.

34) (New.) The method of claim 32 wherein the first DAC is a N-bit DAC in the memory device, the second DAC is an M-bit DAC in the memory device and the DAC value is an m most significant bits of the first DAC provided by the memory controller, wherein M is less than N.

35) (New.) The method of claim 32 wherein the first DAC and the second DAC are binary weighted control DACs in the memory device.

36) (New.) The method of claim 32 wherein the memory device is a DRAM device.

37) (New.) The method of claim 32 wherein the output driver is associated with a pin in the memory device.

38) (New.) The method of claim 32 wherein the receiving the calibration signal comprises:

measuring the calibration signal to obtain a count value; and,

dividing the count value to obtain the calibration value.

39) (New.) The method of claim 32 wherein the providing a calibration signal comprises applying a data signal to a gate of transistor coupled to a current source.

40) (New.) The method of claim 32 wherein the providing a calibration signal comprises transferring the calibration signal to the memory device.

41) (New.) A method for calibrating a memory device output driver comprising:

providing a calibration value to a first DAC coupled to a first output pin in a memory device;

providing a calibration value to a second DAC coupled to a second output pin in the memory device;

outputting a first current from a third DAC in response to an initialization value;

outputting a first bias current to the first DAC in response to the first current; and,

outputting a second bias current to the second DAC in response to the first current.

42) (New.) The method of claim 41 wherein the first DAC is coupled to a first output driver coupled to a first current source and the second DAC is coupled to a second output driver coupled to a second current source.

43) (New.) The method of claim 41 further comprising:

receiving the first bias current by a first transistor coupled to the first DAC; and,

receiving the second bias current by a second transistor coupled to the second DAC.

44) (New.) The method of claim 41 wherein the first DAC, second DAC and third DAC are binary weighted control DACs.

45) (New.) The method of claim 41 wherein the memory device is a DRAM device.

46) (New.) The method of claim 41 wherein the providing a calibration value to a first DAC includes providing the calibration value to the first DAC by a memory controller and the providing a calibration value to a second DAC includes providing a calibration value to a second DAC by the memory controller.

47) (New.) The method of claim 41 further comprising:

obtaining a DAC value associated with the first DAC;

applying the DAC value to the third DAC;

outputting a second current from the third DAC in response to the DAC value;

outputting a third bias current to the first DAC in response to the second current; and,

outputting a fourth bias current to the second DAC in response to the second current.

48) (New.) The method of claim 47 wherein the first DAC is an N-bit DAC and the DAC value is an m most significant bits of first DAC.